Claims:

1. A processor designed to operate in a plurality of modes for processing vector and scalar instructions, where a vector instruction identifies a single operation to be performed on a plurality of data elements, and a scalar instruction identifies a single operation to be performed on a single data element, comprising:

one or more register files for storing scalar and vector data;

a parallel vector unit coupled to receive data from the one or more register files and comprising a plurality of functional units configurable to operate in a vector operation mode and a scalar operation mode, the parallel vector unit including means for tightly coupling a plurality of the functional units to perform an operation specified by a current instruction;

wherein under a vector operation mode the parallel vector unit performs, in parallel, a single vector operation on a plurality of data elements, the operations performed on the plurality of data elements each being performed by a different functional unit of the parallel vector unit; and

wherein under a scalar operation mode the parallel vector unit performs a scalar operation on a data element received from the one or more register files in a functional unit within the parallel vector unit.

2. The processor of claim 1, wherein the parallel vector unit includes a mode selector which reads a mode identifier associated with each instruction and causes the parallel vector unit to enter vector operation mode or scalar operation mode depending on the value of the mode identifier

3. The processor of claim 1, further including a power savings unit which disables functional units not used for processing a given instruction.

4. The processor of claim 3, wherein the functional units are disabled by disabling their clock input signals.

5. The processor of claim 3, wherein the functional units are disabled by disabling their supply voltage.

6. The processor of claim 3, wherein the power savings unit disables unused functional units during scalar operations.

7. The processor of claim 1, further comprising means for designating one or more functional units necessary for execution of an instruction as preferred slots.

8. The processor of claim 7, wherein the means for designating includes an issue/branch unit, coupled to the parallel vector unit, including means for reading an instruction and determining what functional units are necessary for performing the instruction, and designating such units as preferred slots.

9. The processor of claim 7, wherein the means for designating includes a tag associated with each datum stored in the one or more register files indicating whether the datum is valid or invalid data, and enable tag logic coupled to the one or more register files, wherein each tag, if set, causes the enable tag logic to cause one or more functional units to be active for processing an instruction.

10. The processor of claim 7, wherein the preferred slots are designated at system design.